## Penumarthi Bhanu Sai Surya Teja

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## Career objective

Secure a responsible career opportunity to fully utilize my training and skills, while making a significant contribution to the success of the company.

## Education

* B.Tech (67%) Electronics and Communication (JNTUK) -2018
* Diploma (71%) Electronics and Communication (SBTET)-2014
* S.S.C (79%) (Board of secondary education) -2010

## Technical skills

* Fundamental concepts and technique used in digital electronics**.**
* Design Electronic Circuits and Developing
* **Computer Language** : Basics of C
* **Hardware Language** : VHDL, Verilog
* Designing Tools : Multi sim 13.0

Xilinx ISE 14.7

Questa SIM 10.0

MATLAB R2010a

* Other Software Skills : MS Office, Photoshop, Windows OS

## PROJECT

Title:Fault Tolerant Parallel FFTs using Error Correction Codes and Parseval Checks

Description:

The aim of project is to decrease the soft errors in the system by using these two techniques. Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. The aim of error tolerant design is to protect parallel FFTs from errors.

## Roles and Responsibilities:

* Gathered the resources required to build the design.
* Performed the single block testing for PARSEVALS CHECKS.
* Performed unit testing for ECC.
* Assembled main blocks using small blocks

## Extra-Curricular & Co-Curricular activities:

* Participated in two days workshop on basics of MATLAB and hands on practice in Analog Communication organized by Sasi institute of technology and engineering Tadapalligudem
* Participated as a sub organizer in Techno cultural fest-2017 organized by Sasi institute of technology and engineering Tadapalligudem

## Hobbies

* Watching movies
* Listening Music

## Strengths

* Flexibility and Adaptability to new environment

## Declaration

I hereby declare that all the above information is true and correct to best of my knowledge.

**Date:**

**Place: Signature**